Description

The SLVU2.8-8-SB is in an SO-8 package and may be used to protect four high-speed line pairs. The layout of the device minimizes trace inductance and reduces voltage overshoot associated with ESD events. The low clamping voltage of the SLVU2.8-8-SB minimizes the stress on the protected IC. The SLVU2.8-8-SB complies with the IEC 61000-4-2 (ESD) standard with ±30kV air and ±30kV contact discharge. The SLVU2.8-8-SB features integrated low capacitance compensation diodes that reduce the maximum capacitance to 1.4pF per line. This, combined with low leakage current, means signal integrity is preserved in high-speed applications such as 10/100/1000 Ethernet.

Features

- Protects four line pairs(eight lines)
- High peak pulse currentl
- Comprehensive pin out for easy board layout
- Low capacitance
- Low leakage current
- Low operating and clamping voltages
- Complies with following standards:
  - IEC 61000-4-2 (ESD) immunity test

    Air discharge: ±30kV

    Contact discharge: ±30kV
  - IEC61000-4-4 (EFT) 40A (5/50ns)
  - IEC61000-4-5 (Lightning) 30A (8/20μs)
- RoHS Compliant

Applications

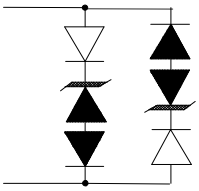
- 10/100/1000 Ethernet

Caution:
This Device is designed for signal line protection only. Not intended to be used under bias, not for application with a power line.

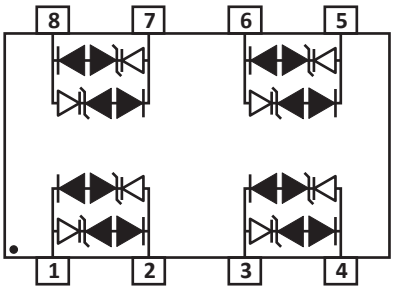
Mechanical Characteristics

- Package: SO-8
- UL Flammability Classification Rating 94V-0
- Terminal Connections: See Diagram Below

Dimensions and Pin Configuration

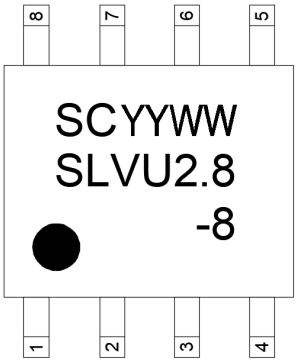


Each Line



Circuit and Pin Schematic

Marking Information



YYWW=Date Code
Dot denotes Pin1

Ordering Information

Part Number	Marking	Packaging	Reel Size
SLVU2.8-8-SB	SC YYWW SLVU2.8-8	2500/Tape & Reel	13 inch

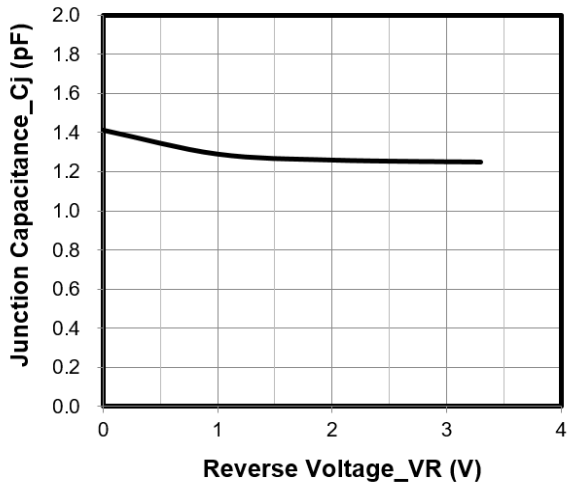
Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power(8/20μs)	Ppk	350	W
Peak Pulse Current(8/20μs)	I_{PP}	30	A
ESD per IEC 61000−4−2 (Air) ESD per IEC 61000−4−2 (Contact)	V_{ESD}	±30 ±30	kV
Operating Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	Tstg	−55 to +150	°C

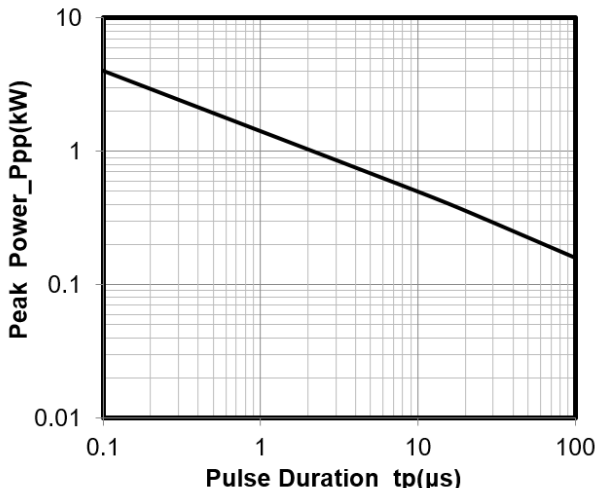
Electrical Characteristics (T_A=25°C unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	V_{RWM}			2.8	V	
Punch-Through Voltage	V_{PT}	3.0			V	I_T = 2μA
Snap-Back Voltage	V_{SB}	0.8			V	I_T = 50mA
Reverse Leakage Current	I_R			0.1	μA	V_{RWM} = 3.3V
Clamping Voltage	V_C		6	9	V	I_{PP} = 10A (8 x 20μs pulse)
Clamping Voltage	V_C		9	12	V	I_{PP} = 30A (8 x 20μs pulse)
Junction Capacitance	C_J		1.4		pF	VR = 0V, f = 1MHz

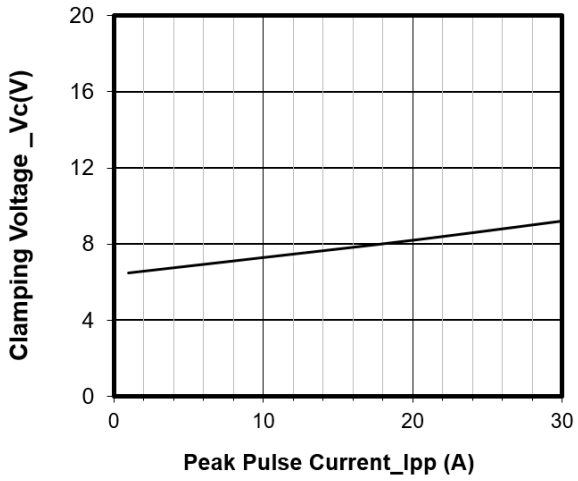
Typical Performance Characteristics (TA=25°C unless otherwise Specified)



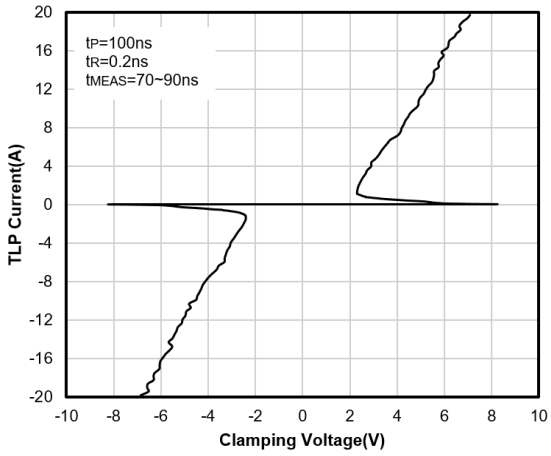
Junction Capacitance vs. Reverse Voltage



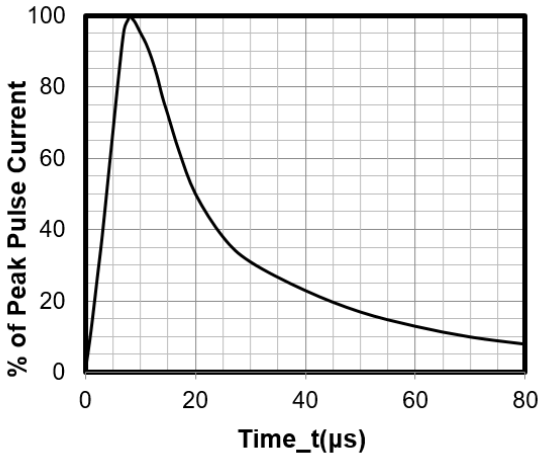
Peak Pulse Power vs. Pulse Time



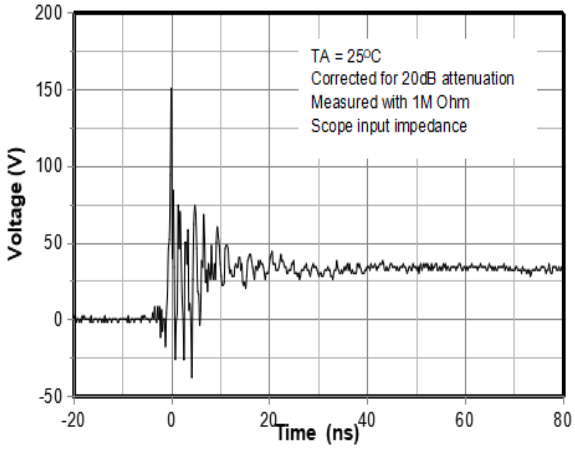
Clamping Voltage vs. Peak Pulse Current



TLP Curve



8 X 20µs Pulse Waveform



ESD Clamping Voltage

8 kV Contact per IEC61000−4−2

Applications Information

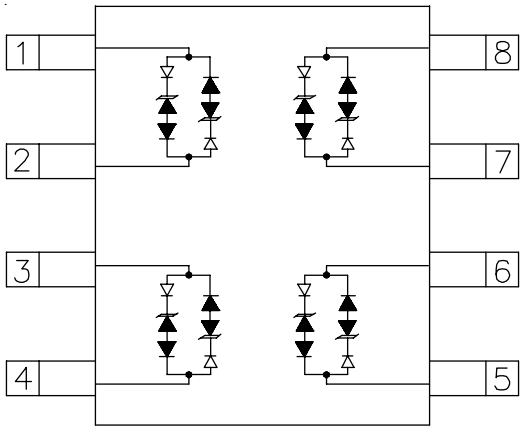
Device Connection for Protection of Eight Data lines

Electronic equipment is susceptible to transient disturbances from a variety of sources including: ESD to an open connector or interface, direct or nearby lightning strikes to cables and wires, and charged cables “hot plugged” into I/O ports. The SLVU2.8-8-SB is designed to protect sensitive components from damage and latch-up which may result from such transient events. The SLVU2.8-8-SB can be configured to protect four high-speed line pairs differentially, or four lines to ground (common mode). The device is connected as follows:

1. **Differential Protection of four line pairs:**

   Line pairs are connected at pins 1 and 2, 3 and 4, 5 and 6, and 7 and 8.

SLVU2.8-8-SB Circuit Diagram

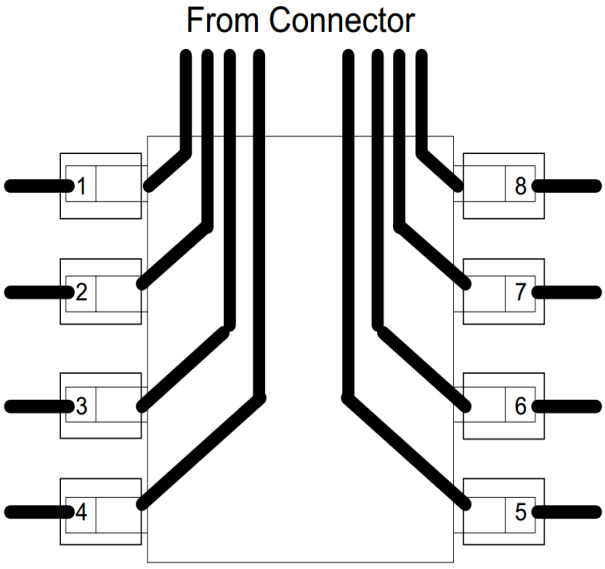


Circuit Board Layout Recommendations for Suppression of ESD.

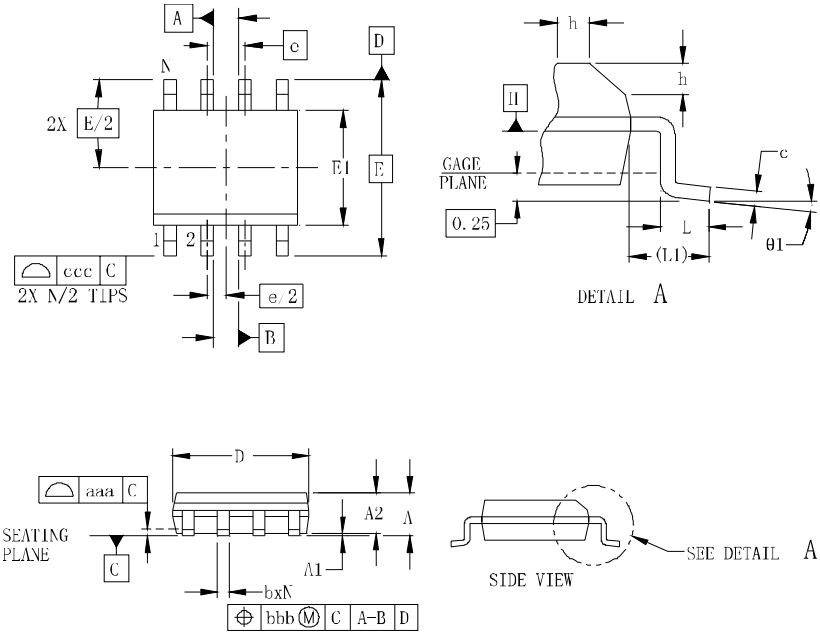
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the device near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

Differential Protection of Four Line Pairs

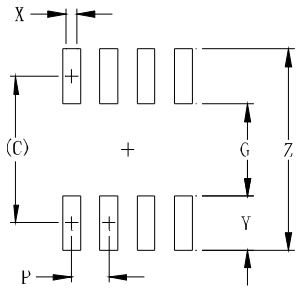


SO-8 Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.25		1.65	0.049		0.065
b	0.31		0.51	0.012		0.020
c	0.17		0.25	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E1	3.80	3.90	4.00	0.150	0.154	0.157
E	6.00 BSC			0.236 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25		0.50	0.010		0.020
L	0.40	0.72	1.04	0.016	0.028	0.041
L1	(1.04)			(0.041)		
N	8			8		
θ1	0°		8°	0°		8°
aaa	0.10			0.004		
bbb	0.25			0.010		
ccc	0.20			0.008		

Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
C	(5.20)	0.205
G	3.00	0.118
P	1.27	0.050
X	0.60	0.024
Y	2.20	0.087
Z	7.40	0.291

Contact Information

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